ABSTRACT OF THE DISCLOSURE

A method of processing signals of a timing controller of a liquid crystal display module, wherein the signals are processed according to a rising edge or a falling edge of a synchronizing signal to generate the control signals for the liquid crystal display module, the control signals including start vertical signals STV(including STV1 and STV2) and gate-on enable signals OE. Then, the gate clock signal CPV, STV1, STV2, and OE pause to be outputted.